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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,920	03/26/2004	Ching-Yu Chang	67,200-1262	9385

7590 09/27/2006

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1756	

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,920	CHANG, CHING-YU	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levinson et al. (6,984,475) in view of Ker et al. (US 20050051848 A1) or Hsu (5,585,299).

The claimed invention is directed to an ESD-resistant photomask and method of preventing mask ESD damage. The ESD-resistant photomask includes a mask substrate, a pattern-forming material provided on the substrate, a circuit pattern defined by exposure regions etched in the pattern-forming material, and positive or negative ions implanted into the mask substrate throughout ion implantation regions. The ions in the ion implantation regions dissipate electrostatic charges on the mask, thus preventing the buildup of electrostatic charges, which could otherwise attract image-distorting particles to the mask or damage the mask.

The applicant discusses the limitations of the prior art in that problems inherent in the conventional use of multiple ESD eliminators mounted beneath the ceiling of the cleanroom is that many areas in the cleanroom lack sufficient downflow of air to facilitate sufficient transfer of the neutralizing ions from the ESD eliminators to the surfaces of the reticles. This increases the likelihood of ESD-induced damage to the reticles as they are

carried or transported from the reticle stocker to the step-and-scan system and as they await their turn for the step-and-scan procedure. Accordingly, a novel ESD-resistant photomask and method of preventing ESD-induced damage to a photomask is needed.

Levinson et al. teach an extreme ultraviolet (EUV) lithography mask - wherein (col. 9, lines 30-40) the substrate 112, or at least the area of the substrate 112 defining the recess 114, can be implanted or impregnated with ions, molecules or compounds to locally increase the conductivity of the substrate 112. For example, the thinned portion 116 can be implanted with ions such as indium, phosphorous, gallium, boron or arsenic, to name a few. The thinned portion 116 can be located adjacent the periphery of the substrate 112 or in another strategically selected location to avoid introducing distortions in the EUV pattern 30 reflected by a mask formed from the mask blank 110.

The teachings of Levinson et al. differ from those of the applicant in that the applicant teaches the use of positive or negative ions implanted into the mask substrate throughout ion implantation regions for the purpose of ESD protection.

Ker et al. teach a method of manufacturing a semiconductor device having a first and second transistor respectively of an electrostatic discharge protection circuit and internal circuit, the method comprising the steps of: providing a substrate;

forming gates of the first and second transistor on the substrate; depositing a mask layer and patterning the mask layer using one single mask to remove the mask layer on the gates, a portion of a drain region of the first transistor, and a source and drain region of the second transistor; implementing a first ion implantation with a first concentration under the masking of the patterned mask layer; removing the mask layer and forming sidewall

spacers of the gates; and implementing a second ion implantation with a second concentration, wherein the concentration of the second implantation is heavier than that of the first implantation.

And wherein the first ion implantation is Nsup- type ESD implantation or Psup- type ESD implantation.

Hsu teaches a process for fabricating an electrostatic discharge (ESD) protective device on a silicon substrate, comprising the following steps of:

1) defining a functional region and an ESD protective region on the silicon substrate and forming a field oxide layer therebetween; (2) forming a gate electrode on the silicon substrate and exposing surfaces of the silicon substrate where the functional region and a source/drain electrode in the silicon substrate are to be formed, then performing an ion implantation process to the exposed surfaces so as to form a lightly doped region;

(3) forming an oxide layer on both the functional region and the ESD protective region;

(4) coating a first photoresist layer on the oxide layer on the ESD protective region and then using an ESD mask for pattern definition so as to form a lightly doped source/drain electrode on the functional region, then removing the first photoresist layer on the oxide layer in the ESD protective region;

(7) ion implanting using the gate electrode in the ESD protective region as mask to form heavily doped region, then removing the second photoresist layer on the functional region.

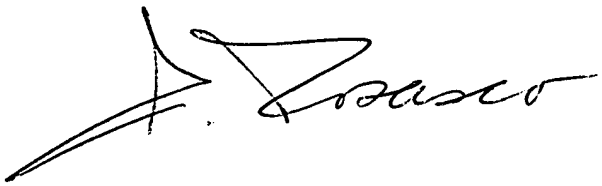
And wherein in Step (2) the ion implantation process uses a source of N-type phosphor ions.

It would have been obvious to one having ordinary skill in the art to take the teachings of Levinson et al. and combine them with the teachings of Ker et al. or Hsu in order to make the claimed invention because Ker et al. or Hsu teach the claimed invention for semiconductor substrates including ion implantation into regions of the substrate for ESD protection and Levinson et al. also teach the implantation of ions into recesses of the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco
Primary Examiner
Art Unit 1756

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09/20/06